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6 an embedded processor configured to control the integrated circuit, the  
7 embedded processor configured to control the interface circuit to receive information  
8 therefrom; and  
9 an array processor for performing arithmetic calculations, the array  
10 processor coupled to the interface circuit to receive information therefrom and connected  
11 to the embedded processor via an internal bus;  
12 wherein the array processor comprises:  
13 a first multiply/accumulator (MAC) unit coupled to a first local  
14 memory, the first local memory comprising a first plurality of operands;  
15 a second MAC unit coupled to a second local memory, the second  
16 local memory comprising a second plurality of operands; and  
17 a first shared operand unit coupled to the first MAC unit and the  
18 second MAC unit for simultaneously providing a first shared operand to the first MAC  
19 unit for computing a first result in association with the first plurality of operands and to  
20 the second MAC unit for computing a second result in association with the second  
21 plurality of operands; and  
22 wherein the first result and the second result are computed  
23 independently of each other; and  
24 wherein the array processor further comprises:  
25 a second shared operand unit coupled to a third MAC unit and a  
26 fourth MAC unit for providing a second shared operand to the third MAC unit and the  
27 fourth MAC unit.

1 10. (Amended) An integrated circuit using a memory, said  
2 integrated circuit comprising:  
3 an interface circuit configured to control access to said memory, said  
4 interface circuit coupled to said memory;  
5 an embedded processor configured to control said integrated circuit, said  
6 embedded processor receiving information from said interface circuit; and

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7 an array processor for performing mathematical calculations on data  
8 received from said interface circuit and connected to said embedded processor via an  
9 internal bus, said array processor comprising:  
10 a plurality of multiplier/accumulator circuits; and  
11 a plurality of shared operand circuits coupled to said plurality of  
12 multiplier/accumulator circuits for simultaneously providing a shared operand to at least  
13 two of said plurality of multiplier/accumulator circuits.

23 21. (New) An integrated circuit comprising:  
2 a first embedded processor;  
3 a first array processor coupled to the first embedded processor;  
4 a first memory interface circuit coupled to the first embedded processor  
5 and the first array processor;  
6 a first communication port coupled to the first embedded processor;  
7 a second communication port configured to communicate with the first  
8 communication port;  
9 a second embedded processor coupled to the second communication port;  
10 a second array processor coupled to the second embedded processor; and  
11 a second memory interface circuit coupled to the second embedded  
12 processor and the second array processor.

24 22. (New) The integrated circuit of claim 21 wherein the array  
2 processor comprises:  
3 a first MAC unit coupled a first local memory; and  
4 a second MAC unit coupled to a second local memory.

25 23. (New) An integrated circuit comprising:  
2 a first embedded processor;  
3 an array processor coupled to the first embedded processor;

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4 a memory interface circuit coupled to the first embedded processor and the  
5 array processor;  
6 a first communication port coupled to the first embedded processor,  
7 wherein the array processor comprises:  
8 a first MAC unit coupled to a first local memory;  
9 a second MAC unit coupled to a second local memory; and  
10 a shared operand unit coupled to the first MAC unit and the second  
11 MAC unit, the shared operand unit for simultaneously providing a shared operand to the  
12 first MAC unit and the second MAC unit.

1 ~~26~~ 24. (New) The integrated circuit of claim ~~25~~ wherein the first  
2 communication port communicates with a second communication port, the second  
3 communication port coupled to a second embedded processor.